REMARKS

Claims 1-29 were examined. All claims were rejected. In response to the above-identified Office Action, Applicants do not amend any claims, cancel any claims, or add any new claims. Reconsideration of the rejections in light of the following remarks is requested.

I. Preliminary Observations

Applicants note that there is a significant potential for confusion in the terminology used for Universal Serial Bus (USB) systems. Specifically, the word "interrupt" has at least two meanings that must be carefully separated. The first meaning is as an adjective, to describe one of the four types of data transfers that may occur over a USB. (The other types are "Isochronous," "Control," and "Bulk.") As noted in the Intel *Universal Host Controller Interface (UHCI) Design Guide*, Revision 1.1 ("*UHCI*"), the Interrupt transfer type is adapted to perform "[s]mall, spontaneous data transfers from a device. The Interrupt transfer type supports devices that require a predicable service interval but do not necessarily produce a predictable flow of data." (*See UHCI*, § 1.1.) From a hardware perspective, Bulk, Control and Interrupt transfers operate *identically* (*UHCI* § 3.4.1.3).

The second meaning of "interrupt" is as a noun or a verb, and relates to the process by which a processor's stream of execution may be paused (often temporarily) to perform some (often brief) higher-priority work. In keeping with this second meaning, it is common to speak of an external device interrupting the processor by asserting a signal, or of the processor performing some sequence of actions in response to an interrupt.

To make matters worse, the hardware circuits that implement USB communications (and therefore the circuits that perform Interrupt transfers, as well as Isochronous, Control and Bulk transfers) can also assert a traditional interrupt signal to cause a CPU to execute a special service routine. In this response, Applicants will attempt to distinguish these two meanings clearly.

II. Claims Rejected Under 35 U.S.C. § 103(a)

The Examiner rejected claims 1-4, 6 and 7 under 35 U.S.C. § 103(a) as unpatentable over U.S. Patent No. 5,802,318 issued to Murray *et al.* ("*Murray*") in view of Intel Corporation, *Universal Host Controller Interface (UHCI) Design Guide* (*supra*, "*UHCI*"). *Murray* discloses a method of operating a USB keyboard connected to a personal computer system. The method emulates a traditional PS/2 keyboard for the benefit of legacy software applications that are not capable of interacting with the USB controller and keyboard in their native mode. The Examiner identifies a number of the elements of claim 1 among the teachings of *Murray*, and relies on *UHCI* to connect *Murray*'s polling with the periodic interrupt caused by an external bus support component as recited in claim 1. However, Applicants respectfully submit that the connection rests on the incorrect assertion of equivalence between "Interrupt" as an adjective describing a USB transfer, and "interrupt" as a noun describing a signal to affect a CPU.

USB Interrupt transfers (as well as Control and Bulk transfers) are performed by a host controller ("HC") under the direction of transfer descriptors ("TD"). The TDs are linked together into queues, and the queues are linked to one or more of 1,024 frames that the HC processes sequentially (one frame per millisecond). (*See UHCI* §§ 1.2 and 3.4, and Figures 3, 9 and 10). When the HC processes a TD for a keyboard (or other "Interrupt transfer") device, it issues a token to the device and waits for data to arrive. (*See UHCI* § 3.4.1.1, 10-step algorithm on p. 28, particularly steps 4 and 6.) If the device has no data to send, it will respond to the token with a negative acknowledgement ("NAK") packet. (*See, e.g.*, http://www.pulsewan.com/data101/usb_basics.htm#interrupt_transfer or *Universal Serial Bus Specification*, Rev. 2.0, § 8.5.4 for more information.) This procedure is properly called "polling," as the Examiner describes, because the HC requests data from the device periodically, without regard to whether the device has data to transmit. Furthermore, this is the normal operational mode of a USB host controller performing Interrupt transfers. Note that no interrupts (in the second sense of the word) are necessary to trigger any part of this process. Once the HC has been configured and started (which is the task of "[s]oftware that is run early in the boot process," *UHCI* § 5.1), it simply loops over and over the array of frame pointers processing the TDs it finds there.

Thus, Applicants respectfully submit that the Examiner errs by asserting that "devices such as USB keyboards are polled, *or interrupt driven*, at a periodic interval." (January 26, 2005 Office Action, p. 3, emphasis added). In the scenario described by *Murray* and that contemplated by *UHCI*, Interrupt transfers (in the first sense of the word) occur *without* interrupts (in the second sense). *Murray* does not teach or suggest at least the element of an external bus support component to cause a periodic interrupt to be generated and to provide support for external bus enable devices responsive to the periodic interrupt, so claim 1 is distinguishable from the references of record for at least that reason.

As to claims 2-4, 6 and 7, those claims depend upon claim 1, and are patentable for at least the reasons discussed in support of that claim. Applicants respectfully request that the Examiner withdraw the rejections of these claims as well.

The Examiner rejected claims 8-12, 14-17, 19 and 23 under 35 U.S.C. § 103(a) as unpatentable over *Murray* (*supra*) in view of *UHCI* (*supra*), and further in view of U.S. Patent No. 6,128,732 issued to Chaiken ("*Chaiken*"). Each of those claims requires an interrupt to be periodically generated. As discussed at some length in regard to claim 1, the claimed interrupt is of the second sort: a signal that causes a processor to pause its execution of a current instruction stream and to execute alternate instructions for servicing a higher-priority need. The Examiner's analyses with respect to each of these claim sets (those based upon independent claim 8 and those based upon independent claim 14) concede that *Murray* fails to teach a periodic interrupt, and incorporate the same erroneous reliance on *UHCI*, where that reference invites confusion between the two meanings of "interrupt." Furthermore, *Chaiken* is only relied upon for a subordinate point regarding memory allocation, and Applicants have been unable to locate any teaching or suggestion of the claimed periodic interrupts. Thus, for reasons similar to those discussed above, Applicants submit that claims 8-12, 14-17, 19 and 23 are patentable over the references of record and request that these rejections be withdrawn.

The Examiner rejected claims 20 and 21 under 35 U.S.C. § 103(a) as unpatentable over *Murray* (*supra*), *UHCI* (*supra*) and *Chaiken* (*supra*), and further in view of U. S. Patent No. 6,772,252 issued to Eichler, Jr. *et al.* ("*Eichler*"). Claims 20 and 21 depend directly or indirectly upon claim 14, as discussed above, and *Eichler* does not supply the missing information about periodic interrupts. Thus, Applicants respectfully submit

that claims 20 and 21 are also patentable over the references of record, and request that these rejections be withdrawn.

Regarding claim 22, the Examiner rejected that claim under 35 U.S.C. § 103(a) as unapatentable over *Murray* (*supra*), *UHCI* (*supra*) and *Chaiken* (*supra*) as applied to its base claim (claim 14), and further in view of *Universal Serial Bus PC Legacy Compatibility Specification* ("*USBLegacy*"). As discussed above in relation to independent claim 1, and reiterated in relation to independent claims 8 and 14, claim 22 incorporates the periodic interrupts that are not taught or suggested by the first three references, and neither the Examiner's analysis nor Applicants' review have uncovered the missing information in *USBLegacy*. Thus, claim 22 is also allowable over the references of record, and Applicants respectfully request that the rejection be withdrawn.

The Examiner rejected claims 24-28 under 35 U.S.C. § 103(a) as unpatentable over *Murray* (*supra*), *UHCI* (*supra*) and *Chaiken* (*supra*), and further in view of U.S. Patent No. 6,560,702 to Gharda *et al.* ("*Gharda*"). However, independent claim 24 and its dependent claims 25-28 all include the element of causing an interrupt to be periodically generated. This element has been shown to be absent from *Murray*, *UHCI* and *Chaiken*, and *Gharda* allegedly teaches only a different element of claim 24 (regarding "re-flashing" of flash ROM). Therefore, claims 24-28 are patentable at least because the element of causing an interrupt to be periodically generated has not been identified in the references.

The remaining claims, 5, 13, 18 and 29, stand rejected under 35 U.S.C. § 103(a) as unpatentable over *Murray* (*supra*), *UHCI* (*supra*) and *Chaiken* (*supra*) as applied to claims 8 and 14, and over *Murray* (*supra*), *UHCI* (*supra*), *Chaiken* (*supra*) and *Gharda* (*supra*) as applied to claim 24, and further in view of Intel Corporation, *Instantly Available Power Managed Desktop PC Design Guide*, Rev. 1.2 ("*IAPM*"). These claims depend upon one of claims 1, 8, 14 or 24, and are patentable for at least the reasons discussed above in support of those base claims, insofar as *IAPM* is not relied upon to supply the missing information regarding periodic interrupts, and Applicants' review of the reference does not suggest that the information is present.

CONCLUSION

In view of the foregoing, it is believed that all claims now pending, namely claims 1-29, patentably define the subject invention over the prior art of record, and are in condition for allowance and such action is earnestly solicited at the earliest possible date. If the Examiner believes that a telephone conference would be useful in moving the application forward to allowance, the Examiner is encouraged to contact the undersigned at (310) 207-3800.

Respectfully submitted,

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Dated: 3/23, 2005

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Marilyn Bass — March 23, 2005